Table 1 - TIME STAMPING HARDWARE MODULE

- **Time Stamping Hardware Module is a dual SPARTAN 6 FPGA based module developed for REAL TIME, HIGH RESOLUTION TIME STAMPING & COUNTING OF [NUCLEAR DETECTOR TYPE] RANDOM OR EXPONENTIAL DISTRIBUTED INPUT LOGIC PULSES AND FOR ANALOG DATA ACQUISITION.**
- **The module operates in two modes: PC mode and Standalone mode.**
- **In PC pulse mode, TTL pulse data from 4 separate channels is time stamped and sent to PC.**
- **In PC analog mode, analog input data acquired from single channel is sent to PC via USB2.0 interface for storage and offline processing.**
- **In Standalone pulse mode, pulse counts in predefined time interval is displayed on the LCD in a channel-wise manner.**
- **In Standalone analog mode, analog input and analog output values are displayed on the LCD as well are also outputted on the analog output connectors.**
- **In Pulse mode, The pulse pair resolution is settable from 5ns to 5us.**
- **In Pulse mode, The pulse counting time is user settable from 1us to 1000s.**
- **In Analog mode, 2 KV Isolated +/ -10V, 1MSPS ADC and +/ -10V, 1MSPS DAC interface for analog input and outputs**
- **In Pulse mode, 4 Channel upto 10MHz input pulse rate, 5ns resolution pulse pair resolution based Random Pulse Acquisition can be done in a seamless manner.**
- **Continuous data storage via USB interface for several hours @ 100Mbps**
- **GPIO and LEDs.**
- **LAB WINDOWS based PC side UI for data storage, processing.**

THIS

HAS BEEN DEVELOPED FOR BARC, MUMBAI FOR REACTOR INSTRUMENTATION APPLICATION